ARGUMENTS/REMARKS

STATUS OF CLAIMS

Claims 1 – 19 are pending.

Claims 1 – 2 are withdrawn from consideration.

Claims 3 – 19 stand rejected.

No claims have been amended

Rejection of claims 3, and 7-11 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,030,852 (Higashisaka)

Claims 3 and 7-11 stand rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent No. 5,030,852 (Higashisaka).

The rejection is respectfully traversed on the grounds that Higashisaka fails to disclose or suggest each limitation of the rejected claims.

As to claim 3, the rejection is traversed on the grounds that Higashisaka fails to disclose at least the limitations of any of: an enhancement mode pHEMT transistor; a depletion mode pHEMT transistor, or a power pHEMT transistor. Claim 3 requires that each of these types of transistors be formed on a single substrate. Higashisaka does not even mention pHEMT transistors of any type. There is a passing reference to HEMT transistors, as well as HBT and RHET, in col. 1, lines 23-31 of Higashisaka. Higashisaka states that "transistor fabrication using these advanced processes" (i.e., HEMT, HBT and RHET) "is currently under development and are not yet available on a commercial basis." Clearly, Higashisaka does not contemplate the use of even HEMT transistors in the described circuits, let alone pHEMT transistors.

By way of background, a pHEMT, or pseudomorphic high electron mobility transistor, is a type of field effect transistor (FET), and more specifically a type of high electron mobility transistor (HEMT). In a HEMT there is a doped donor/undoped spacer layer of one material and an undoped channel layer of a different material. A heterojunction is formed between the doped donor/undoped spacer layer and the undoped channel layer. The doped donor layer has a wider bandgap than the undoped channel layer. Due to the conduction band discontinuity at the heterojunction, electrons are injected from the doped donor/undoped spacer layer into the undoped channel layer. Thus, electrons from the relatively large bandgap donor layer are transferred into the relatively narrow bandgap channel layer where they are confined to move only in a plane parallel to the heterojunction. In a pHEMT transistor, one or more of the layers incorporated into the device has a lattice constant which differs slightly from the lattice constants of other materials of the device. As noted above, Higashisaka indicates that HEMT transistors are not yet commercially available, and does not mention the claimed pHEMT transistors at all.

Furthermore, there is no disclosure or reference to power transistors of any type, let alone power pHEMT transistors, in Higashisaka. The Examiner points to col. 7, lines 21-25 and col. 9, lines 20-27, as disclosing power pHEMT transistors. A power pHEMT is a depletion mode pHEMT characterized by higher drain operating voltage than a conventional depletion mode pHEMT. While an enhancement mode transistor is disclosed in Higashisaka at col. 7, lines 25-26, and a depletion type transistor is disclosed in Higashisaka at col. 9, lines 20-27, there is no disclosure of

power transistors. Accordingly, the cited portion of Higashisaka discloses neither a pHEMT transistor nor a power transistor.

In view of the complete absence in Higashisaka of any disclosure or suggestion of the claim limitations discussed above, claim 3 is allowable.

Claim 7 is an independent claim reciting an analog to digital converter, having an enhancement mode pHEMT device, a depletion mode pHEMT device, and a power pHEMT device on a single substrate. As discussed above in connection with claim 3, Higashisaka does not teach pHEMT devices of any description, and does not teach power transistors of any description. Accordingly, claim 7 is allowable.

Claims 8 and 9 depend from claim 7, and are allowable at least by virtue of their dependency from an allowable base claim.

Claim 10 is an independent claim that includes all of the limitations of claim 3, and is allowable at least for the reasons that claim 3 is allowable.

Claim 11 depends from claim 10, and is allowable at least by virtue of its dependency from an allowable base claim.

In view of the foregoing remarks, it is respectfully requested that the rejection of claims 3 and 7-11 be withdrawn.

Rejection of claims 4-6 and 12-19 under 35 U.S.C. 103(a) as being unpatentable over Higashisaka in view of Newman, et al. (U.S. Patent No. 5,705,940).

The standard for a *prima facie* case of obviousness is the following:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable

> expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. . . . *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

MPEP §2142.

As to claim 4, the rejection is respectfully traversed, for at least the reasons that (1) the references cited by the Examiner, even when combined, do not teach or suggest an integrated circuit having all of the limitations of claim 4; and (2) the motivation asserted by the Examiner would not cause one of ordinary skill in the art to modify the principal reference as proposed by the Examiner.

The Examiner cites col. 7, lines 39-62 of Newman as teaching the following limitations of claim 4:

a. an analog input for electrical signals in communication with at least one of the first block, the second block, and the third block;
b. a clock input in communication with at least one of the first block, the second block, and the third block; and
c. a digital output for electrical signals in communication with at least one of the first block, the second block, and the third block;
d. wherein the first block, the second block, and the third block connect to form an analog to digital converter.

However, the cited section of Newman does not even teach an analog to digital converter; instead, this section of Newman discusses D/A (digital to analog) converters. Accordingly, the combination of references as proposed by the Examiner does not teach an integrated circuit having all of the limitations of claim 4.

The motivations asserted by the Examiner would not motivate one of ordinary skill in the art to modify the principal reference in the manner proposed. The Examiner states that "it would have been obvious to one having ordinary skill

in the art at the time the invention was made to modify the teachings of Higashisaka (accordance with the teaching of Newman) to form a transistor since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art." This statement is nothing more than an improper statement that the modification is within the capability of one of ordinary skill in the art.

> A statement that modifications of the prior art to meet the claimed invention would have been "'well within the ordinary skill of the art at the time the claimed invention was made'" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).

MPEP 2143.01(IV). Indeed, the case relied upon by the Examiner, *St. Regis Paper Co. v. Bemis Co.*, 549 F.2d 843, 193 U.S.P.Q. 8 (7th Cir. 1977), *cert. denied*, 434 U.S. 833, 98 S. Ct. 119, 54 L. Ed. 2d 94 (1977), as a Seventh Circuit case, is not binding precedent in the Office, and furthermore, is not good law. The *St. Regis Paper Co.* opinion relies on the discredited "synergistic combination" standard, stating: "the Lokey bag is only entitled to a patent if the fusion of the old elements that comprised the Poppe patent and the old element of multiple layering created a synergistic combination." 549 F.2d at 838. The use of the "synergistic combination" standard has never been approved by the Federal Circuit, and indeed, was rejected by the Seventh Circuit a mere two years after *St. Regis Paper Co.* in *Republic Industries, Inc. v. Schlage Lock Co.*, 592 F.2d 963, 971 (7th Cir. 1979) ("Because synergism centers exclusively on the performance of the elements after combination and without regard to the obviousness or nonobviousness of making

the combination, synergism does not comport with the Graham mandate to apply section 103.") Accordingly, the Examiner's reliance on *St. Regis Paper Co. v. Bemis Co.* is improper.

The Examiner further states that "doing so would facilitate the manufacture of the semiconductor device and enhance the performance of the transistor." However, the Examiner does not explain either how the proposed modification would facilitate the manufacture of the semiconductor device of Higashisaka or enhance the performance of the transistors of Higashisaka. Indeed, as claim 4 contains limitations to a digital-to-analog converter, modifying Higashisaka to create a digital-to-analog converter would neither facilitate the manufacture of the semiconductor device nor improve the speed of the transistors.

As noted above, Higashisaka fails to disclose pHEMT transistors of any description, and Newman does nothing to remedy this deficiency of Higashisaka.

In short, the Examiner has failed to provide a proper prima facie case of obviousness as to claim 4.

For this reason, as well as the reasons set forth above in connection with claim 3, claim 4 is allowable over the prior art of record.

Claim 5 depends from claim 3, and is allowable at least by virtue of its dependence from an allowable base claim.

Claim 6 depends from claim 3, and adds the further limitation that the integrated circuit is capable of operating at a frequency within the range of from very low frequency up to and including X-band frequencies. In order for this limitation to be taught in the

prior art, a reference must teach a circuit capable of operating at this entire frequency range; a circuit capable of operating at only a portion of this range does not teach the limitations of claim 6. The cited portion of Newman, namely col. 2, lines 30-34, does not teach a circuit capable of operating over this entire frequency range. Accordingly, the references as combined fail to teach all of the limitations of claim 6. For at least this reason, as well as the reasons set forth above in connection with claim 3, claim 6 is allowable.

Claims 12-13 depend from claim 3, and are allowable at least by virtue of their dependence from an allowable base claim.

Claim 14 depends from claim 3, and also recites a double recess. The Office Action fails to identify any portion of either of the cited references which teaches a double recess. Accordingly, there is no proper prima facie case of obviousness as to claim 14. For at least this reason, in addition to its dependency from an allowable base claim, claim 14 is allowable.

Claim 15 depends from claim 3, and is allowable at least by virtue of its dependence from an allowable base claim.

Claim 16 depends indirectly from claim 3, and further recites that the recess of the power pHEMT transistor is a double recess, the recess of the depletion mode pHEMT transistor is a single recess, and each of said recesses is defined through at least one common layer of said substrate. There is no teaching or suggestion in either of the cited references of a power pHEMT transistor having a double recess and a depletion mode pHEMT transistor having a single recess, each of those recesses defined through at least one common layer of a substrate. Accordingly, the references

as combined fail to teach all of the limitations of claim 16. For at least these reasons, as well as the reasons set forth above in connection with claim 3, claim 16 is allowable.

Claims 17-19 depend directly or ultimately from claim 3, and are allowable at least by virtue of their dependency from an allowable base claim.

CONCLUSION

Applicant believes he has addressed all outstanding matters, and respectfully requests that claims 3 – 19 be allowed.

Should there be any questions or outstanding matters, the Examiner is cordially invited and requested to contact Applicant's undersigned attorney at his number listed below.

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